



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,088	01/29/2004	Andrew T. Tomerlin	CML01079J	4603

7590 03/09/2005

Larson & Associates, P.C.
221 East Church Street
Frederick, MD 21701-5405

EXAMINER

LUU, AN T

ART UNIT	PAPER NUMBER
----------	--------------

2816

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AR

Office Action Summary

Application No.

10/767,088

Applicant(s)

TOMERLIN ET AL.

Examiner

An T. Luu

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| <p>1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1-29-04</u>.</p> | <p>4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.</p> <p>5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</p> <p>6) <input type="checkbox"/> Other: _____.</p> |
|--|--|

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3 and 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3, the limitation "the control processor", line 2, lacks antecedent basis.

In claims 8 and 9, the limitation "the configurable circuits" lacks antecedent basis.

In claim 10, the limitation "the program control command", line 2, lacks antecedent basis.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6-10, 17-24 and 26-27 are rejected under 35 U.S.C. 102(b) as being anticipated by the Yokota et al reference (U.S. Patent 5,712,582).

Yokota et al discloses in figure 1 an apparatus comprising a variable length delay line 100, the delay line having an input and having N delay elements (D1-m) to provide a plurality of N delayed outputs as shown; the variable length delay line having a number of active delay

Art Unit: 2816

elements determined by a program command (select signal); and a configurable processing array 130 receiving the delayed outputs from the active delay elements and secondary processing data (delay data), the configurable processing array comprising an array of configurable circuit elements (G1-m) as required by claim 1.

As to claim 2, figure 1 shows a control processor 160 that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements.

As to claim 3, figure 1 shows a control processor 160 controlling the delay of the N delay elements.

As to claim 4, figure 1 shows a delay locked loop 100 controlling the delay of the N delay elements.

As to claim 6, figure 1 shows the configurable processing array comprising an input (output of 400) and output (output of OR gate) that can be configured under a program control (selector control and decoder 160).

As to claim 7, figure 1 shows the configurable processing array comprising a plurality of outputs (output of G1-m) that can be configured under a program control (selector control and decoder 160).

As to claim 8, figure 1 shows the apparatus comprising a plurality of configurable processing unit (G1-m).

As to claim 9, figure 1 shows the apparatus comprising a programmable logic device 160.

Art Unit: 2816

As to claim 10, the apparatus comprising a programmable MUX (i.e., decoder 160) responsive to a command (delay data) to selectively enable a selected group of delay elements while disabling remaining delay elements (i.e., which tap output is selected).

As to claims 17-21, they are rejected for reciting method/step derived from the apparatus of claims 1, 2, 3, 6, 8 and 9 which are rejected as noted above.

As to claim 22, figure 1 discloses a plurality of N delay elements (D1-m) with each delay having an input and an output, the N delay elements being coupled together in series output to input to form a delay line; a programming input (input terminal of 160) that receives a program control command (delay data); and a programmable multiplexer 160, responsive to the program control command to selectively enable a selected group of delay elements while disabling remaining delay elements (i.e., which tap output is selected).

As to claim 23, figure 1 shows a delay control input (output of 174) for controlling the delay of the N delay elements.

As to claim 24, figure 1 show the delay line is controlled by an output of the delay locked loop 100.

As to claims 26 and 27, the scopes of these claims are similar to that of claims 23 and 24. Therefore, they are rejected for the same reason set forth above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2816

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5, 11-15, 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yokota et al reference (U. S. Patent 5,712,58) in view of the Lee reference (U.S. Patent 5,901,190).

Yokota et al discloses all the claimed invention except for disclosing a delay element comprising a pair of series connected inverters as required by claims 5, 25 and 28.

Lee discloses in figure 4 a delay line comprising delay elements having a pair of series connected inverters (FUD1-n) as required by the claims.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Lee into that of Yokota since a buffer is known to be implemented in many different ways.

A skilled artisan would be motivated to employ a delay comprising two series connected inverters since it would provide a minimized phase difference between tapped outputs.

As to claim 11, the scope of claim is similar to the combination of claims 1, 2, 4 and 5. Therefore, it is rejected for the same reason set forth above.

As to claim 12, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 6. Therefore, it is rejected for the same reason set forth above.

As to claim 13, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 7. Therefore, it is rejected for the same reason set forth above.

As to claim 14, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 8. Therefore, it is rejected for the same reason set forth above.

Art Unit: 2816

As to claim 15, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 9. Therefore, it is rejected for the same reason set forth above.


Conclusion


7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
2-25-05 


TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800